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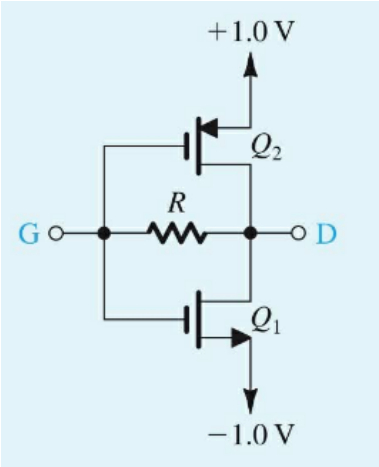
Problem 1. **(1 point)**
The MOSFETs in the circuit of Fig. 1 are matched, having $k'_n(W/L)_1 = k'_p(W/L)_2 = 1\,\text{mA/V}^2$ and $|V_t| = 0.5\,\text{V}$. The resistance $R = 1\,\text{M}\,\Omega$.



(a) For G and D open, what are the drain currents I_{D1} and I_{D2}?

I_{D1} = _____ mA

I_{D2} = _____ mA

(b) For $r_o = \infty$, what is the voltage gain of the amplifier from G to D? (Hint: Replace the transistors with their small-signal models.)

Voltage gain from G to D = _____ V/V

(c) For finite r_o ($|V_A| = 20\,\text{V}$), what is the voltage gain from G to D and the input resistance at G?

Voltage gain from G to D = _____ V/V

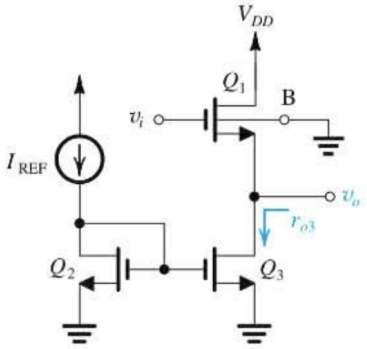
Input resistance at G = _____ kΩ

(d) If G is driven (through a large coupling capacitor) from a source v_{sig} having a resistance of $20\,\text{k}\,\Omega$, find the voltage gain v_d/v_{sig}.

v_d/v_{sig} = _____ V/V

Problem 2. **(1 point)**
A source follower for which $k'_n = 200\,\mu A/V^2$, $V'_A = 20\,V/\mu m$, $\chi = 0.15$, $L = 0.5\,\mu m$, $W = 20\,\mu m$, and $V_t = 0.6\,V$ is required to provide a dc level shift (between input and output of $0.9\,V$.)

What must the bias current be? Find g_m, g_{mb}, r_o, A_{vo}, and R_o. Assume that the bias current source has an output resistance equal to r_o. Also find the voltage gain when a load resistance of $2\,k\Omega$ is connected to the output.



Bias current = _____ mA

g_m = _____ mA/V

g_{mb} = _____ mA/V

r_o = _____ $k\Omega$

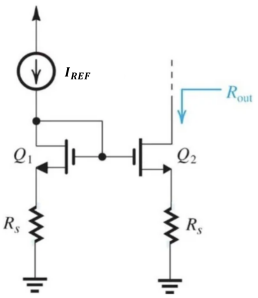
A_{vo} = _____ V/V

R_o = _____ $k\Omega$

Voltage gain with $R_L = 2\,k\Omega$: _____ V/V

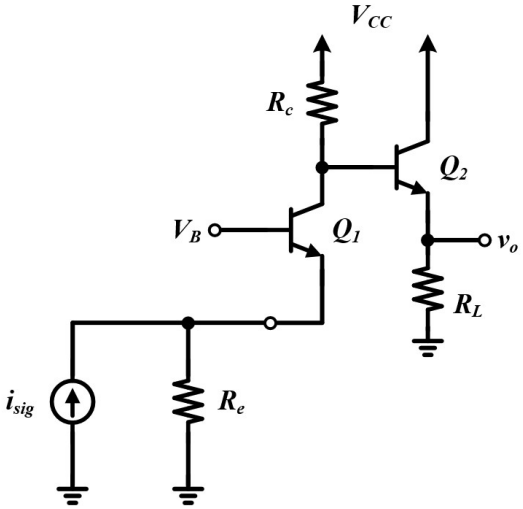
Problem 3. **(1 point)**
Figure shows a current source realized using a current mirror with two matched transistors Q_1 and Q_2.
Two equal resistances R_s are inserted in the source leads to increase the output resistance of the current source.

Given the following parameters:
$I_{REF} = 100\mu A$, $g_m = 2.5mA/V$, $V_A = 5V$
The maximum allowed dc voltage drop across R_s is $0.2V$.
Assume that the voltage at the common-gate node is approximately constant.
Find the maximum available output resistance R_{out} of the current source.



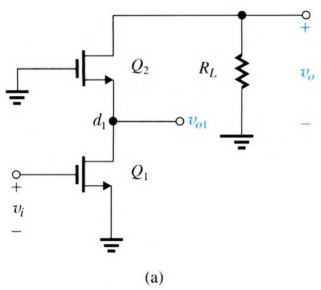
R_{out} = _____ $k\Omega$

Problem 4. **(1 point)**
Find the gain v_o/i_{sig} for the case
$g_{m1} = 2.3\ mS$
$g_{m2} = 2.2\ mS$
$\beta_1 = 116.1$
$\beta_2 = 87.7$
$R_e = 1.1\ k$
$R_c = 3.6\ k$
$R_L = 2\ k.$
(neglect channel-length modulation)



v_o/i_{sig}= _____

Problem 5. **(1 point)**



A CMOS cascode amplifier is shown in the figure above. Both transistors Q_1 and Q_2 are identical and are biased at a DC current $I = 0.2$ mA.
The given parameters for the ideal calculations are:
$\mu_n C_{ox} = 400\ \mu\text{A/V}^2$
$W/L = 5.4\mu\text{m}/0.36\mu\text{m}$
$V_A' = 5\ \text{V}/\mu\text{m}$

Part 1: Theoretical Calculation
Calculate the required load resistor R_L so that the overall voltage gain $A_v = \frac{v_o}{v_i}$ is exactly -118 V/V. What is the voltage gain of the common-source stage (the Q_1 stage)?
(R_o R_{in2} is used the approximate formula to calculate and Assume the transistors are operating in the saturation region).

$R_L =$ _____ kΩ

$A_{v1} =$ _____ V/V

Part 2: PSpice Simulation Assignment
In this part, you will verify the circuit using a real device model in PSpice. Due to the nonlinear characteristics of real transistors, the simulated gain will differ from your ideal calculation.

Instructions:
1. Build the circuit in PSpice using the NMOS0P18 provided in moodle for both Q_1 and Q_2 .You will only modify the parameter of the R_L, other parameter just use its default value.
2. Use an ideal DC voltage source to provide the VDD voltage $V = 3.3$ V, gate voltage of Q1 is $Vdc = 0.6$ V

$Vac = 1$ V,gate voltage of Q2 is $Vdc = 1.5$ V
3. Set the resistor R_L to the exact value you calculated in Part 1

4. Perform an AC Sweep simulation.
5. Measure the voltage gain $\frac{v_o}{v_i}$ $\frac{v_{o1}}{v_i}$

Submission:
Please take screenshots of:
- Your PSpice schematic .
- The AC sweep plot showing the gain $\frac{v_o}{v_i}$ $\frac{v_{o1}}{v_i}$.