

assignment1

closes March 26, 2026, 11:59:00 PM CST

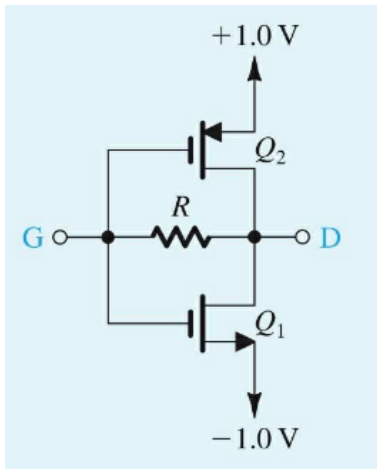
(E24131186)

Section: 1142_E227020_2

This PDF is available for convenience. Assignments must be submitted within **WeBWorK** for credit.

Problem 1. (1 point)

The MOSFETs in the circuit of Fig. 1 are matched, having $k'_n(W/L)_1 = k'_p(W/L)_2 = 1 \text{ mA/V}^2$ and $|V_t| = 0.5 \text{ V}$. The resistance $R = 1 \text{ M}$.



(a) For G and D open, what are the drain currents I_{D1} and I_{D2} ?

$$I_{D1} = \text{_____ mA}$$

$$I_{D2} = \text{_____ mA}$$

(b) For $r_o = \infty$, what is the voltage gain of the amplifier from G to D ? (Hint: Replace the transistors with their small-signal models.)

$$\text{Voltage gain from } G \text{ to } D = \text{_____ V/V}$$

(c) For finite r_o ($|V_A| = 20 \text{ V}$), what is the voltage gain from G to D and the input resistance at G ?

$$\text{Voltage gain from } G \text{ to } D = \text{_____ V/V}$$

$$\text{Input resistance at } G = \text{_____ k}$$

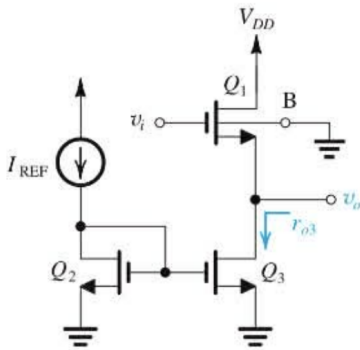
(d) If G is driven (through a large coupling capacitor) from a source v_{sig} having a resistance of 20 k , find the voltage gain v_d/v_{sig} .

$$v_d/v_{sig} = \text{_____ V/V}$$

Problem 2. (1 point)

A source follower for which $k'_n = 200 \mu A/V^2$, $V'_A = 20 V/\mu m$, $\chi = 0.15$, $L = 0.5 \mu m$, $W = 20 \mu m$, and $V_t = 0.6 V$ is required to provide a dc level shift (between input and output of $0.9 V$.)

What must the bias current be? Find g_m , g_{mb} , r_o , A_{vo} , and R_o . Assume that the bias current source has an output resistance equal to r_o . Also find the voltage gain when a load resistance of $2 k\Omega$ is connected to the output.



Bias current = _____ mA

$g_m =$ _____ mA/V

$g_{mb} =$ _____ mA/V

$r_o =$ _____ k Ω

$A_{vo} =$ _____ V/V

$R_o =$ _____ k Ω

Voltage gain with $R_L = 2 k\Omega$: _____ V/V

Problem 3. (1 point)

Figure shows a current source realized using a current mirror with two matched transistors Q_1 and Q_2 .

Two equal resistances R_s are inserted in the source leads to increase the output resistance of the current source.

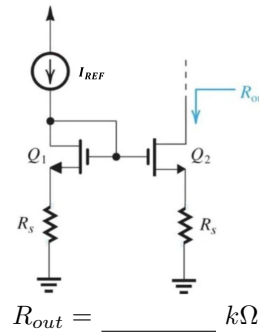
Given the following parameters:

$I_{REF} = 115 \mu A$, $g_m = 1.8 mA/V$, $V_A = 5 V$

The maximum allowed dc voltage drop across R_s is $0.2 V$.

Assume that the voltage at the common-gate node is approximately constant.

Find the maximum available output resistance R_{out} of the current source.



$R_{out} =$ _____ k Ω

Problem 4. (1 point)

Find the gain v_o/i_{sig} for the case

$$g_{m1} = 4.2 \text{ mS}$$

$$g_{m2} = 2.8 \text{ mS}$$

$$\beta_1 = 97.8$$

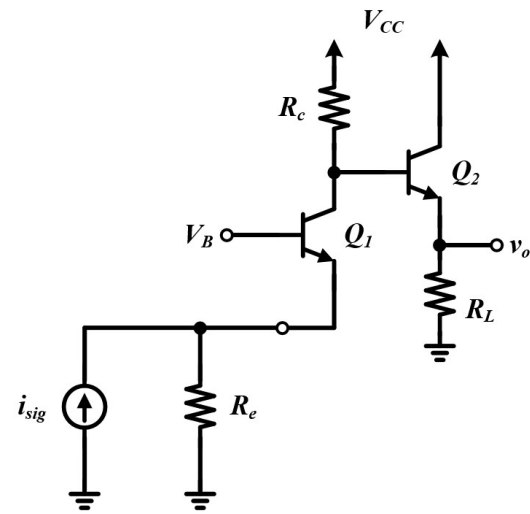
$$\beta_2 = 92.9$$

$$R_e = 1.1 \text{ k}$$

$$R_c = 2.1 \text{ k}$$

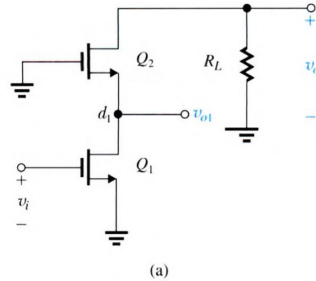
$$R_L = 2.9 \text{ k}.$$

(neglect channel-length modulation)



$$v_o/i_{sig} = \underline{\hspace{2cm}}$$

Problem 5. (1 point)



A CMOS cascode amplifier is shown in the figure above. Both transistors Q_1 and Q_2 are identical and are biased at a DC current $I = 0.2 \text{ mA}$.

The given parameters for the ideal calculations are:

$$\mu_n C_{ox} = 400 \text{ } \mu\text{A}/\text{V}^2$$

$$W/L = 5.4 \text{ } \mu\text{m}/0.36 \text{ } \mu\text{m}$$

$$V'_A = 5 \text{ V}/\mu\text{m}$$

Part 1: Theoretical Calculation

Calculate the required load resistor R_L so that the overall voltage gain $A_v = \frac{v_o}{v_i}$ is exactly -98 V/V . What is the voltage gain of the common-source stage (the Q_1 stage)?

(R_o R_{in2} is used the approximate formula to calculate and Assume the transistors are operating in the saturation region).

$$R_L = \underline{\hspace{2cm}} \text{ k}\Omega$$

$$A_{v1} = \underline{\hspace{2cm}} \text{ V/V}$$

Part 2: PSpice Simulation Assignment

In this part, you will verify the circuit using a real device model in PSpice. Due to the nonlinear characteristics of real transistors, the simulated gain will differ from your ideal calculation.

Instructions:

1. Build the circuit in PSpice using the NMOS0P18 provided in moodle for both Q_1 and Q_2 . You will only modify the parameter of the R_L , other parameter just use its default value.
2. Use an ideal DC voltage source to provide the VDD voltage $V = 3.3 \text{ V}$, gate voltage of Q_1 is $V_{dc} = 0.6 \text{ V}$

$V_{ac} = 1$ V, gate voltage of Q2 is $V_{dc} = 1.5$ V

3. Set the resistor R_L to the exact value you calculated in Part 1

4. Perform an AC Sweep simulation.

5. Measure the voltage gain $\frac{v_o}{v_i}$ $\frac{v_{o1}}{v_i}$

Submission:

Please take screenshots of:

- Your PSpice schematic .
- The AC sweep plot showing the gain $\frac{v_o}{v_i}$ $\frac{v_{o1}}{v_i}$.